Reg. No:

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech I Year II Semester Supplementary Examinations March-2021
DIGITAL LOGIC DESIGN
(Common to CSE & CSIT)

Time: 3 hours   Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1   a   i) $(615)_{10} = (\quad)_{16}$ ii) $(214)_{10} = (\quad)_8$ iii) $(0.8125)_{10} = (\quad)_2$ **6M**

     b   Obtain the Complement & Dual of Boolean Expression   **6M**
       i. $A+B+A'B'C$ ii. $AB + A(B+C) + B'(B+D)$

OR

2   Explain about complements with examples?   **12M**

UNIT-II

3   a   Explain NAND- NOR implementations?   **8M**
     b   Simplify the Boolean expression using K-map?   **4M**
       $F(A,B,C,D,E) = \sum m(0,1,4,5,16,17,21,25,29)$

OR

4   Obtain the minimal product of sums and design using NAND gates   **12M**
    $F(A,B,C,D) = = \sum m(0,2,3,6,7) + d(8,10,11,15)$

UNIT-III

5   a   Design a 4 bit adder-subtractor circuit and explain the operation in detail.   **6M**
     b   Explain about Priority encoder?   **6M**

OR

6   a   What is combinational circuits and explain analysis and design procedure of combinational circuits.   **5M**
     b   Explain the functionality of a Multiplexer?   **7M**

UNIT-IV

7   a   Explain the Logic diagram of SR flip-flop?   **6M**
     b   Explain about ripple counter.   **6M**

OR

8   a   What is state assignment? Explain with a suitable example?   **7M**
     b   Write the differences between latches and flip flops?   **5M**

UNIT-V

9   What is memory decoding? Explain about the construction of 4 X 4 RAM?   **12M**

OR

10   Implement the following function using PLA   **12M**
    $A(x,y,z) = \sum m(1,2,4,6)$ $B(x,y,z) = \sum m(0,1,6,7)$ $C(x,y,z) = \sum m(2,6)$

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